COLUMBIA ENGINEERING | Electrical Engineering

EE/CISL Seminar

Columbia University Electrical Engineering Department
&
Columbia Integrated Systems Lab

Ajay Balankutty

Principal Engineer, Intel

Date: Friday, April. 18
Time: 2:00 pm - 3:00 pm
Location: EE conference room, 13th Floor
Seminar: Architecting High-Speed SerDes Transceivers in Advanced CMOS Technologies
Host: Peter R. Kinget

Electrical Engineering & Columbia Integrated Systems Lab Seminar Series

Architecting High-Speed SerDes Transceivers in Advanced CMOS Technologies

CMOS technology in the angstrom (Å) era of semiconductors continues to provide scaling benefits to digital systems (like CPUs and GPUs) and Analog/Mixed-signal IPs (like PLLs, data converters, wireline and wireless transceivers) by realizing more capable and power efficient designs. As always, a deep understanding of semiconductor and interconnect physics enables circuit designers to differentiate and exploit technology scaling fully. I will give an overview of an advanced CMOS process technology with nanoribbon (RibbonFET) with back-side power delivery, and some of the fundamental physics that that can influence circuit and architecture choices. We will then go over in detail SerDes transceiver trends, architecture advances and circuits evolution paired with CMOS scaling, with specific examples from our recent work in 100Gb/s and 200Gb/s links.

About Ajay Balankutty

Ajay Balankutty received his M.S. and Ph.D. from Columbia University in Electrical Engineering in 2010. He is currently a Principal Engineer, technical lead and manages SerDes development at Intel, where his group in develops the first Serial I/O transceivers in Intel's latest process technology nodes that serves as a reference design for all foundry customers. His pathfinding team also develops the IP architecture and circuits for next generation Ethernet, OIF and PCIe standards. Since 2010, Ajay and his team developed 28Gb/s, 56Gb/s, 112Gb/s and 224Gb/s SerDes transceivers. In addition to SerDes design, he and his team performs system technology co-optimization (STCO) to ensure that CMOS scaling continues to provide benefits for analog/mixed-signal circuits and systems. Ajay has published over 25 papers in peer-reviewed conferences and journals and is a member of the Technical Program Committee of CICC.